JUPITER EUROPA ORBITER MISSION STUDY

MEMORY INVESTIGATION for JUPITER EUROPA ORBITER MISSION

Revision A

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CL#08-4219

MEMORY INVESTIGATION for a EUROPA EXPLORER MISSION CONCEPT

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EXECUTIVE SUMMARY

The Europa Explorer mission concept would present many challenges for which the answers at present are few – specifically in the area of memory to support a proposed Hybrid Data Recorder. Although the amount of data necessary to be stored within the recorder would be non-trivial (approximately 3.5 Gb Non-Volatile and 16 Gb Volatile), the larger challenge would be to locate devices with performance that would be satisfactory during and after exposure to a high radiation environment. This report summarizes the studies pursued, results obtained, and recommendations for further investigation.

1 Task

Architect a data recorder for the proposed Europa Explorer mission with a minimum data capacity of approximately 3.5 Gb of non-volatile data storage and approximately 16 Gb of volatile storage. The recorder shall be capable of an input data rate of 30 Mbps. All non-volatile devices shall operate following exposure to 100 kilorads$_{(Si)}$ total ionizing dose (TID) at the die level.

2 Technologies Investigated

A survey was performed to determine the most suitable technologies and their suppliers for this effort. Non-volatile memory technologies investigated were Flash and Phase Change. Volatile technologies investigated were Static RAM (SRAM) and Dynamic RAM (DRAM & SDRAM).

2.1 Non-Volatile Memory

2.1.1 Flash Memory

Flash memory retains data information by the imposition of an electric charge upon a thin film of silicon oxide literally floating above a single transistor cell. The imposed charge determines whether the transistor is conductive (state 1) or highly resistive (state 0). Due to the generally insulative nature of the oxide and other surrounding elements, the generation of a high voltage (on the order of 20 to 25 Volts) is required – all Flash devices today generate this voltage internally. The method of generation of this high voltage from a low voltage input (typically 1.8 Volts) is highly susceptible to damage caused by

all forms of radiation – heavy ion, proton, and gamma. Based upon this, the use of Flash devices was ruled out for this application.

2.1.2 Phase Change memory

In this technology the physical state of a plastic-like material is changed from an amorphous to crystalline state and back by controlled, direct heating of the memory bit being addressed. The resistance of the material varies by 2-3 orders of magnitude between the two states. This large spread in resistance makes it easy for a sense amp to discern between a One and a Zero data state.

The figure below describes the expected resistance change according to program state.

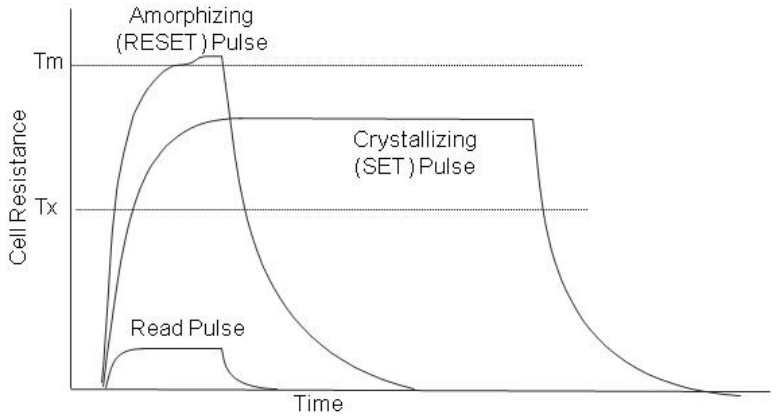

Figure 1 - Phase Change Resistance versus Temperature Profile

Testing has shown that the data storage material is immune to strategic radiation, and therefore is a prime candidate for this application – as increases in radiation tolerance at the device level brings about a decrease in the amount of radiation shielding required.

The densest Phase Change device available today is 4 Mb per die, regardless of the device's radiation capability. The BAE 4Mbit CRAM device, part number 8406746 was selected and procured.

2.1.3 High Density Phase Change

Investigation of literature revealed that Samsung Semiconductor, Korea, was developing high density phase change memory devices. JPL was invited to meet with the Executive Vice President of Technology at Samsung headquarters, Seoul South Korea, April 2008. From JPL, Dr Harald Schone, Dr Douglas Sheldon and Karl Strauss were in attendance. At this meeting, Samsung learned of JPL's anticipated data storage requirements for potential future missions. Samsung presented to JPL five 512 Mbit phase change memory devices (part number KPS1215EZM). Test results are discussed later in this report.

2.2 Volatile Memory

2.2.1 Dynamic Random Access Memory

Dynamic Random Access Memory (DRAM) and its technical cousin Synchronous DRAM (SDRAM) have been available for over thirty years. In a dynamic memory, data is stored on a bit basis as a charge on a capacitive plate. A one, for example, would be interpreted as the plate having a charge above some level; conversely a zero would be interpreted as having a charge below some level. As the capacitors involved are quite small, they do lose their retained charge over time and therefore require a refreshment cycle; often this refresh cycle is performed autonomously by the memory device itself without processor intervention. Due to the very small cell size, the use of DRAM is an ideal solution in developing a high-density recorder. The drawback to the DRAM (and SDRAM) is that the very mechanism used to contain the charge on the capacitor plate makes it especially sensitive to bombardment by gamma radiation and cosmic rays. Currently available test data shows failures below 100 krad. Future vendor specific testing is planned and might allow usage screened parts within the JEO environment with adequate shielding."

The densest SDRAM device available today is 2 Gb per die; a radiation tolerant or radiation hardened DRAM or SDRAM does not exist. Information received from industry partners revealed that one device in particular was showing very good radiation response – more so than other devices of similar design.

3 Testing & Investigation

Two different approaches were taken on the devices being considered. With respect to Phase Change, the BAE device was manufactured as radiation hardened (megarad) on a known radiation hardened foundry; the Samsung device was manufactured by a foundry with no special processing or design for radiation tolerance taken into account. Therefore, investigation of the Phase Change devices manufactured rad-hard was limited to shifts in various parameters from first-on through several hundred cycles of operation. An investigation of device construction was performed.

As the Samsung device was manufactured using high-yield processes, the decision was made to focus on radiation capability.

For both devices, the chemistry requires the application of a large amount of heat to melt that material, upwards of one milliwatt per bit. The figure below shows the two energy states for any particular bit. The high resistance amorphous state has sufficient activation energy as to be susceptible to relaxation into the crystalline state with the application of external heat- resulting in a loss of data.

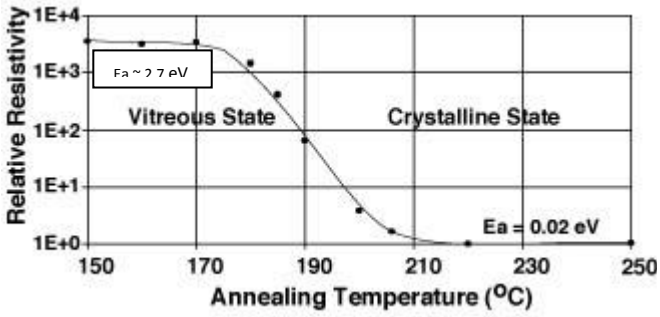

Figure 2 - Activation Energy for Phase Change Material

The SDRAM device was also manufactured on a very high yield line. The investigation was also limited to radiation effects.

3.1 BAE Phase Change

As these devices are, by design and process, radiation hardened, testing was limited to certain parametrics: Retention and Endurance. Further, as the cells require temperatures of approximately 230 Celsius to melt the material, concern exists about the effect of temperature on the surrounding interconnect materials – an electromigration study was performed.

3.2 Samsung Phase Change

As the concern here was more on radiation effects and less on manufacturing quality, investigation was limited to Single Event Effects based on two items: 1) a knowledge base exists wherein these devices are shown to be operational to at least 150 kilorads, and, more importantly 2) a Single Event testing board and software already existed, having been generated by a third party.

3.3 Synchronous DRAM

Similar to the Samsung Phase Change, the concern here was radiation effects. JPL became aware of two important factors: first is that Single Event Effects testing show that the devices do not experience Single-Event induced Latchup (SEL) at levels exceeding 83 MeV, and second, that the devices maintain operation within specification to levels of at least 100 kilorads. As this device set had the potential to be a driver in terms of additional data recorder shielding, additional testing was performed at pre-selected levels between 100 and 500 kilorads.

4 Test Results

4.1 BAE Phase Change

A destructive physical analysis revealed that the BAE CRAM is manufactured on 0.25 μm bulk CMOS using five layers of metal. The SEM microphotograph below shows the unique Phase Change memory cell structure

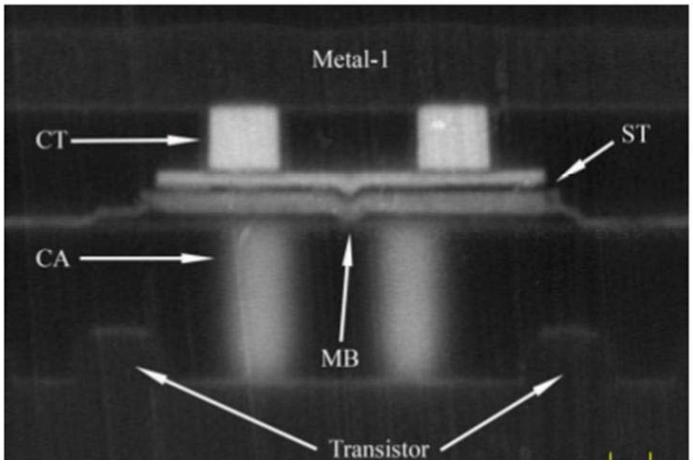

Figure 3 - 35,000x SEM of BAE Memory Cell

As mentioned earlier, the high energy bands of the phase change material bring about a natural instability in the retention of data. It is possible, with sufficient external thermal energy applied, to result in the loss of data.

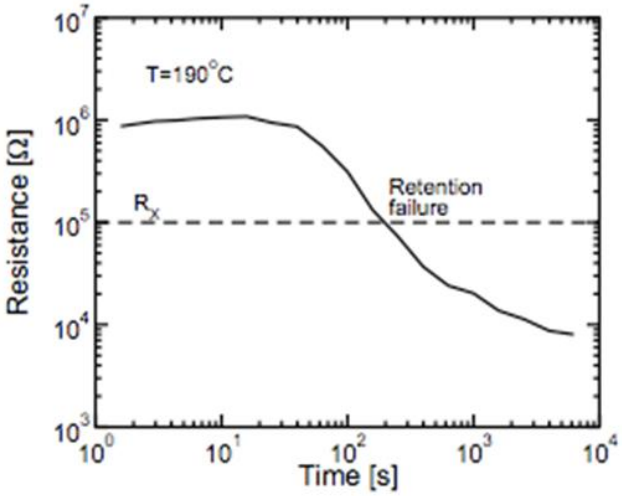

Figure 4 - Data Retention Failure in Phase Change Memory

Knowledge of this susceptibility was used in the design of the Europa Data Recorder, following industry recommendation to avoid powering more than one CRAM device in a stacked configuration.

X-ray Diffraction analysis (performed earlier by sources outside of JPL) show that the most likely cause of operation induced retention failure is the change in stoichiometry of the cell chemistry – that of the three materials used (Gallium, Strontium, and Tellurium), the latter is more likely to migrate to the bottom electrode and form a dendritic growth to the top electrode.

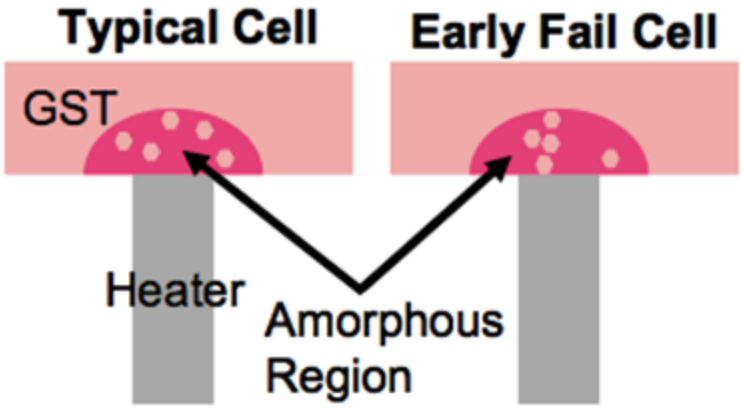

Figure 5 - Early Cell Failure due to Cell Stoichiometry Alteration

Based upon these two effects, BAE has re-designed their Phase Change device to include built-in Error Correcting Code (Hamming) reducing the effective capacity of the offered device from 4Mb to 2Mb. The ECC can be disabled at the time of manufacture thereby restoring the capacity to 4Mb. It is the 4Mb devices without internal ECC that were selected for use on the recorder.

Testing to date by JPL's Electronic Parts organization has revealed that of six devices tested, one has developed total failure of retention across one entire 8-bit word. No analysis has been performed to determine the cause of the failure, but at this is symptomatic of a row access transistor failure as opposed to eight unique circumstances of bit-cell failure. It must be noted that the devices tested were early production evaluation samples and not Process of Record. We are just now in receipt of the POR devices.

4.2 Samsung Phase Change

The difficulty here is that the Samsung devices were delivered as – and are available only in – fully enclosed plastic-epoxy packages. In order to test the devices in a high energy particle beam, the devices were first mounted to a glass-epoxy test carrier and then subjected to high-temperature acid wash, Unfortunately, for one or more reasons which will not be discussed further, all three devices were

destroyed by the acid wash process. A check with Samsung revealed that they have no means in place to specially package the die in ceramic, or retrieve the die after dicing and before encapsulation.

In lieu of the de-encapsulation process destroying three of the samples, a single test was performed at a single Linear Energy Transfer (LET) at Texas A&M University's Cyclotron. A single device was tested at and LET of 28.2 MeV/mg-cm2 from a 25 MeV/u Xe beam. Due to the device fully encapsulated, only a single LET measurement was taken due to range limitation. Although single event upset (SEU) is not a concern for the storage cells, and SEU in the control logic can cause a single event functional interrupt (SEFI). Although the device's SEFI response could not be fully characterized, i.e. a space environment SEFI rate developed, a few types of SEFIs were discovered which will aid in the development of the test infrastructure needed to fully characterize the SEFI error modes. A brief discussion into the test methodology is required to discuss the test results. Two methods of dynamic testing were performed, the first was a "readback only", whereby the device was constantly read out, if large numbers of errors were read out a SEFI was declared and the run ended. After the beam was stopped, the device was reset and a full device readback was performed to ensure no errors persisted. The second dynamic mode consisted of a repeating pattern of reading out the manufacturer ID followed by the reading of incrementing addresses (in both dynamic modes the data written to the device was the address). The important thing to note concerning the second test methodology was that a soft reset was performed every time the manufacturer ID was read out. A few types of SEFI modes were discovered, including all ones or zeros on the output, read ID error, and address error. In most cases, a hard reset fixed the problem. In a single instance, a write had to be performed to remove errors. We do not believe these were upsets to the memory cells themselves, but some kind of control logic SEFI. The device was exposed to a total of 33 krads.

4.3 SDRAM

Additional total dose testing of the SDRAM device shows remarkable results. Testing shows that the devices remain within all parameters monitored up to, and including, 150 krads. Additionally, these devices remained fully functional, although out of specification in terms of current, to 500 kilorads – the top end of the test contracted. The dashed line in the figure indicates the specified maximum device current for the "Self-Refresh" operation.

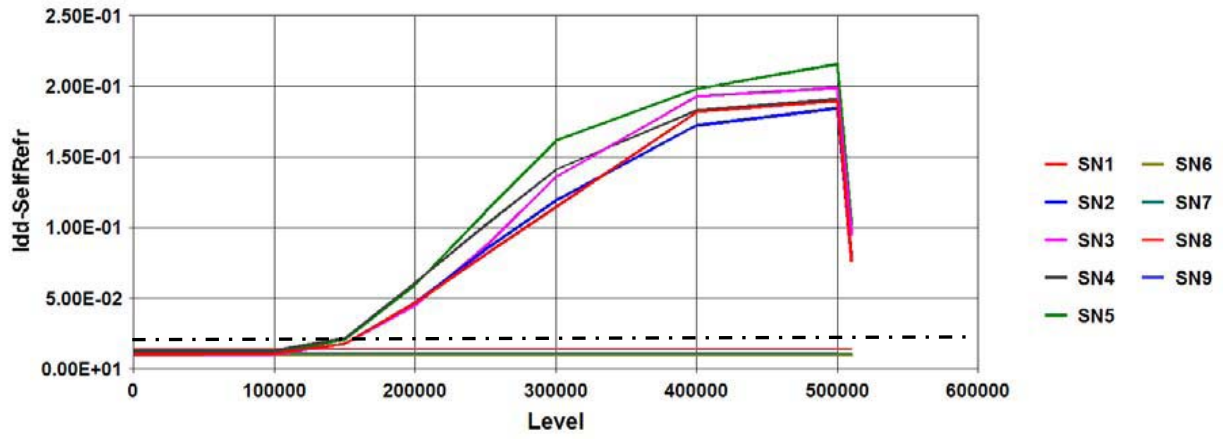

Figure 6 - Idd versus Total Dose - devices 6 thru 9 are non-radiated control samples

The Idd curve shows a return to near-normal limits after two days of unbiased anneal.

5 Testing Conclusion

JPL has experienced one error in six BAE CRAM devices tested. The cause of the error has not been determined; recall that the devices checked were engineering evaluation samples provided as a courtesy to JPL and were unscreened at the factory.

We were not able to fully characterize the high capacity Samsung devices due to test set-up error but we now have knowledge of certain upset modes. Total dose testing on the 2 Gb SDRAM device shows very good performance and confirms operability in the expected data recorder radiation environment.

6 Recommendations

6.1 BAE Phase Change

With fully screened "process of record" devices now at hand, perform data retention and electromigration studies using lessons learned from the previous "pipe cleaner" tests.

6.2 Samsung Phase Change

Work with Samsung and determine if phase change die would be available at the scribed wafer level. In this way, JPL may be able to bond the die into packages that permit ion beam exposure. Future work for these devices include SEFI characterization, single event latchup (SEL) characterization, and total ionizing dose (TID) characterization.

These die represent a density of 128 times that available anywhere else, *the strategic advantage offered by these devices is certainly too large to ignore.*

Additional die are being manufactured. Once received, perform total dose and energetic particle testing to the maximum extent possible. These devices may become a strategic advantage to JPL.

Further, JPL has been invited to participate and present its findings to the next Samsung Technical Innovation Conference, April 2009.

6.3 2Gb SDRAM.

Conduct proton and neutron irradiation. Conduct additional total ionizing dose radiation studies on select other parameters (such as refresh time) to fill-out the known data. Conduct cell-level analysis with manufacturer to determine if radiation response can be designed into other products.